BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

325 48452

SEARCH REQUEST FORM **Scientific and Technical Information Center - EIC2800**

Rev. 11/20/00 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 8/7/01 Serial # 09/645403 Case Priority Date _____

Your Name THANH NGUYEN Examiner # 74457

AU 2813 Phone 308-9439 Room 3B07

In what format would you like your results? Paper is the default. PAPER DISK (EMAIL)

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. Would you like to sit with the EIC searcher in a mediated interactive search? Yes / (No) _____

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: NONE

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. N/A

What types of references would you like? Please checkmark:

Primary Refs ✓	Nonpatent Literature ✓	Other _____
Secondary Refs ✓	Foreign Patents ✓	_____
Teaching Refs ✓		_____

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, elected species, structures, synonyms, keywords, acronyms, registry numbers, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims:

please concentrate in searching for a cleaning an opening/via/hole/contact/viahole by using phosphoric acid containing solution + nitric acid containing solution

BEST AVAILABLE COPY

****

STAFF USE ONLY

Searcher HARRISON
Searcher Phone 306-5429
Searcher Location CP4-9C18
Date Searcher Picked Up 8-7-01
Date Completed 8-7-01
Searcher Prep/Rev Time 60
Online Time 60

Type of Search

Structure (#) _____
Bibliographic X
Litigation _____
Fulltext _____
Patent Family _____
Other _____

Vendors

STN X
Dialog _____
Questel/Orbit _____
Lexis-Nexis _____
WWW/Internet _____
Other _____

FILE 'INPADOC, HCAPLUS, WPIX' ENTERED AT 09:41:35 ON 07 AUG 2001

L1 360 S LI LI ?/AU,IN
L2 1700 S "LI LI"/AU OR "LI LI"/IN OR L1

FILE 'REGISTRY' ENTERED AT 09:43:32 ON 07 AUG 2001

L3 5 S "PHOSPHORIC ACID"/CN OR ("PHOSPHORIC ACID (H10P8O25)"/CN OR "PHOSPHORIC ACID (H332PO4)"/CN OR "PHOSPHORIC ACID (H4P2O5)"/CN OR "PHOSPHORIC ACID (H6P6O18)"/CN)
L4 3 S ("NITRIC ACID"/CN OR "NITRIC ACID (H13NO3)"/CN OR "NITRIC ACID (H2NO3)"/CN OR "NITRIC ACID (HONO2)"/CN)

FILE 'INPADOC, HCAPLUS, WPIX' ENTERED AT 09:47:59 ON 07 AUG 2001

L5 162264 S L3 OR PHOSPHORIC ACID OR NITRIC ACID OR 1724/DRN OR 1711/DRN OR 1970/DRN
L6 15 S L5 AND L2
L7 12822 S L5 AND (RESIDU#### OR CLEAN####)
L8 944 S L7 AND (VIA OR VIAHOLE OR OPENING OR HOLE OR CONTACT)
L9 108034 S L3 OR PHOSPHORIC ACID OR 1711/DRN OR 1970/DRN
L10 65053 S L4 OR NITRIC ACID OR 1724/DRN
L11 58 S L8 AND L9 AND L10
L12 57 S L11 NOT L6
L13 8 S L12 AND (VIA OR VIAHOLE)
L14 20 S L12 AND RESIDU#####
L15 23 S (L13 OR L14)
L16 34 S L12 NOT L15
L17 1071 S L9 AND L10 AND (WASH#### OR CLEAN#### OR RESIDU####)
L18 162 S L17 AND (FL OR FLUORI##### OR F)
L19 171 S L18 OR (L17 AND FLUORO#######)
L20 11 S L19 AND (L6 OR L11)
L21 15 S L19 AND (VIA OR VIAHOLE OR OPENING OR HOLE OR CONTACT)
L22 4 S L21 NOT (L20 OR L6 OR L11)
L23 1 S L19 AND (POLYMER#### OR POLY)(2A)(METAL###### OR OXIDE)
L24 2 S L17 AND MICRON?/PA,CS

FILE 'INSPEC' ENTERED AT 10:12:06 ON 07 AUG 2001

L25 253 S VIAHOLE/TI OR VIA HOLE/TI
L26 1773 S VIAHOLE OR VIA(2A)HOLE
L27 0 S L26 AND NITRIC AND PHOSPHORIC
L28 5 S L26 AND (H/CHI AND N/CHI AND O/CHI)
L29 3 S L26 AND (H/CHI AND P/CHI AND O/CHI)
L30 8 S (L28 OR L29)
L31 5933 S PHOSPHORIC OR (H/CHI AND P/CHI AND O/CHI)
L32 16595 S HNO3 OR NITRIC(2W)ACID OR (H/CHI AND N/CHI AND O/CHI)
L33 1196 S L31 AND L32
L34 40 S L33 AND (VIAS OR VIA HOLE OR VIAHOLE OR THROUGH HOLE OR THROUGHHOLE OR CONTACT##### OR CONDUCT#### PAD OR OPENING OR HOLE)
L35 40 S L34 NOT L30
L36 7 S L35 AND (CLEAN#### OR PRECLEAN##### OR WASH#### OR PREWASH#### OR RESIDU####)

L6 ANSWER 2 OF 15 HCAPLUS COPYRIGHT 2001 ACS
AN 2001:417369 HCAPLUS
DN 135:27883
TI Manufacture and cleaning of a semiconductor to remove metal nitride and oxynitride extrusions from metal silicides which cause short circuits
IN Chen, Gary; *Li, Li* ; Hu, Yongjun
PA USA
SO U.S. Pat. Appl. Publ., 14 pp., Division of U.S. Ser. No. 385,396.
CODEN: USXXCO
DT Patent
LA English
IC ICM H01L021-44
NCL 438655000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2001003061	A1	20010607	US 2000-738796	20001215

PRAI US 1999-385396 A3 19990830

AB Metal nitride and metal oxynitride extrusions often form on metal silicides. These extrusions can cause short circuits and degrade processing yields. The present invention discloses a method of selectively removing such extrusions. In one embodiment, a novel wet etch comprising an oxidizing agent and a chelating agent selectively removes the extrusions from a wordline in a memory array. In another embodiment, the wet etch includes a base that adjusts the pH of the etch to selectively remove certain extrusions relative to other substances in the wordline. Accordingly new metal silicide structures can be used to form novel wordlines and other types of integrated circuits.

IT Cleaning
IT 7697-37-2, *Nitric* *acid* , processes
7722-84-1, Hydrogen peroxide, processes 7727-54-0, Ammonium persulfate 7790-92-3, Hypochlorous acid 7790-93-4, Chloric acid 10028-15-6, Ozone, processes 16068-46-5, Potassium phosphate
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(cleaning agent; manuf. and cleaning of semiconductor to remove metal nitride and oxynitride extrusions from metal silicides which cause short circuits)

L6 ANSWER 4 OF 15 HCAPLUS COPYRIGHT 2001 ACS
AN 2000:635196 HCAPLUS
DN 133:216523
TI Etching dielectric films in semiconductor device fabrication
IN *Li, Li* ; Yates, Don L.
PA Micron Technology, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English

IC ICM C23F001-00
NCL 216099000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 57
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6117351	A	20000912	US 1998-55644	19980406

AB A method for removing a plurality of dielec. films from a supporting substrate by providing a substrate with a second dielec. layer overlying a first dielec. layer, contacting the substrate at a first temp. with a first acid soln. exhibiting a pos. etch selectivity at the first temp., and then contacting the substrate at a second temp. with a second acid soln. exhibiting a pos. etch selectivity at the second temp. The first and second dielec. layers exhibit different etch rates in the first and second acid solns. The first and second acid solns. may contain *phosphoric* *acid* . The first dielec. layer may be silicon nitride and the second dielec. layer may be silicon oxide. Under these conditions, the first temp. may be about 175.degree.. and the second temp. may be about 155.degree..
IT *7664-38-2* , *Phosphoric* *acid* , processes
RL: USES (Uses) etchant; in etching dielec. films in semiconductor device fabrication)

L6 ANSWER 5 OF 15 HCAPLUS COPYRIGHT 2001 ACS
AN 2000:622366 HCAPLUS
DN 133:216457
TI Forming a conductive bonding pad in semiconductor device fabrication
IN Jiang, Tongbi; *Li, Li*
PA Micron Technology, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM C23C022-00
NCL 148240000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 38
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6113709	A	20000905	US 1998-60786	19980415

AB The present invention is drawn to a method of lowering the net resistivity of an interconnect by depositing a monomer layer upon an aluminum bonding pad, the treatment thereof to cross link the monomer to form an elec. conductive polymer, and simultaneously, the substantial redn. of alumina, Al2O3, to metallic aluminum. In the method of the present invention, deposition of a monomer layer in a solvent, volatilization of the solvent, and contact with a strong oxidizer such as a potassium permanganate allows for the use of the strong oxidizer without the hindrance of having to deal with a manganese oxide husk on the surface of the aluminum bonding pad.

Preferably, the chem. qualities of the monomer will include the tendency to be a reducing agent to the native oxide film of the bonding pad. By selecting a monomer that tends to reduce rather than to oxidize, the problem of thickening the native oxide film is avoided. Another preferred chem. quality of the monomer and its polymer after cross linking, is that it will act as a protective coating to the chip package for substantially all further processing. In particular, the monomer or its cross-linked polymer will act as a protective coating to the chip package during an acid dip in an oxidizer soln. such as acidic KMnO4.

IT 64-19-7, Acetic acid, processes 74-90-8, Hydrocyanic acid, processes 463-79-6, Carbonic acid, processes 7601-90-3, Perchloric acid, processes *7664-38-2* , *Phosphoric* *acid* , processes 7664-39-3, Hydrofluoric acid, processes 7697-37-2, *Nitric* *acid* , processes 7782-99-2, Sulfurous acid, processes 10034-85-2, Hydriodic acid 10035-10-6, Hydrobromic acid, processes
RL: USES (acidic medium; in forming conductive bonding pad in semiconductor device fabrication)

L6 ANSWER 7 OF 15 HCAPLUS COPYRIGHT 2001 ACS
AN 2000:31204 HCAPLUS
DN 132:72298
TI Removing residual etch films and formation of interconnections
IN *Li, Li* ; Westmoreland, Donald L.; Yates, Donald L.
PA Micron Technology, Inc., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-302
ICS B08B006-00
NCL 134001300
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6012469	A	20000111	US 1997-932737	19970917
US 6192899	B1	20010227	US 2000-480450	20000110

PRAI US 1997-932737 A1 19970917

AB A method for cleaning polymer film residues from in-process integrated circuit devices is disclosed. Specifically, a method for forming a contact via in an integrated circuit is disclosed in which the formation of a metalization conductive element is exposed through a dry anisotropic etch. During the etch, a polymer film residue forms from masking materials, and coats the newly formed via. The polymer film may have metals incorporated in it from the metalization conductive element. A F-based etchant is used to remove the polymer film. Protection of the metalization conductive element during the cleaning process is accomplished with passivation additives comprising straight, branched, cyclic, and arom. hydrocarbons. Attached to the hydrocarbons are functional groups comprising .gtoreq.3 hydroxyls.

IT *7664-38-2*, *Phosphoric* *acid* , processes
7782-77-6, Nitrous acid
7664-39-3, Hydrogen fluoride, processes
RL: NUU (Nonbiological use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES removal of polymer film residues after etching in integrated circuit fabrication using)

L6 ANSWER 8 OF 15 HCAPLUS COPYRIGHT 2001 ACS
AN 2000:10585 HCAPLUS
DN 132:72248
TI Method for removing silicon nitride in the fabrication of semiconductor devices
IN *Li, Li* ; Wu, Zhiqiang; Hawthorne, Richard C.; Hawthorne, Elvia M.
PA Micron Technology, Inc., USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-30
NCL 438439000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6010949	A	20000104	US 1996-734358	19961021

AB A method for use in the fabrication of semiconductor devices in accordance with the present invention includes providing a Si nitride region and oxidizing a region of material in proximity to the Si nitride region. The Si nitride region is then hydrogenated and thereafter, the hydrogenated Si nitride region is removed. The hydrogenation step may include immersing the Si nitride region into pressurized boiling H2O and/or treating the Si nitride region with pressurized H2O vapor and the removing step includes removing the hydrogenated Si nitride region with hot H3PO4. The method may be used in a LOCOS process. Further, the oxidn. of the material and the hydrogenation of the Si nitride may be performed in the same pressurizable unit.
IT *7664-38-2* , *Phosphoric* *acid* , processes
7732-18-5, Water, processes RL: USES (in removing silicon nitride in fabrication of semiconductor devices)

L15 ANSWER 2 OF 23 HCAPLUS COPYRIGHT 2001 ACS
AN 2000:740920 HCAPLUS DN 134:155145
TI *Clean* solutions to the incoming wafer quality impact on lithography process yield limits in a dynamic copper/low-k research and development environment
AU Lysaght, Patrick S.; Ybarra, Israel; Sax, Harry et al. SEMATECH Inc., Austin, TX
SO Proc. SPIE-Int. Soc. Opt. Eng. (2000), 3998(Metrology, Inspection, and Process Control for Microlithography XIV), 284-293. CODEN: PSISDG; ISSN: 0277-786X
AB The continued growth of the semiconductor manufg. industry has been due,

in large part, to improved lithog. resoln. and overlay across increasingly larger chip areas. Optical lithog. continues to be the mainstream technol. for the industry with extensions of optical lithog. being employed to support 180 nm product and process development. While the industry momentum is behind optical extensions to 130 nm, the key challenge will be maintaining an adequate and affordable process latitude (depth of focus/exposure window) necessary for 10% post-etch crit. dimension (CD) control. If the full potential of optical lithog. is to be exploited, the current lithog. systems can not be compromised by incoming wafer quality. Impurity specifications of novel Low-k dielec. materials, plating solns., chem.-mech. planarization (CMP) slurries, and chem. vapor deposition (CVD) precursors are not well understood and more stringent control measures will be required to meet defect d. targets as identified in the National Technol. Roadmap for Semiconductors (NTRS). This paper identifies several specific poor quality wafer issues that have been effectively addressed as a result of the introduction of a set of flexible and reliable wafer back surface *clean* processes developed on the SEZ Spin-Processor 203 configured for processing of 200 mm diam. wafers. Patterned wafers have been back surface etched by means of a novel spin process contamination elimination (SpCE) technique with the wafer suspended by a dynamic nitrogen (N2) flow, device side down, *via* the Bernoulli effect. This paper addresses a no. of direct and immediate benefits to the MicraScan III deep-UV (DUV) step-and-scan system at SEMATECH. These enhancements have resulted from the resoln. of three significant problems: (1) back surface particle/ *residual* contamination, (2) wafer flatness, and (3) control of contaminant materials such as copper (Cu). Data assocd. with the SpCE process, optimized for flatness improvement, particle removal, and Cu contamination control is presented in this paper, as it relates to excessive consumption of the usable depth of focus (UDOF) and comprehensive yield enhancement in photolithog. Addnl., data illustrating a highly effective means of eliminating copper from the wafer backside, bevel/edge, and frontside edge exclusion zone (0.5 mm - 3 mm), is presented. The data, obtained within the framework of std. and exptl. copper/low-k device prodn. at SEMATECH, quantifies the benefits of implementing the SEZ SpCE *clean* operation. Furthermore, this data confirms the feasibility of utilizing existing (non-copper) process equipment in conjunction with the development of copper applications by verifying the reliability and cost effectiveness of SpCE functionality.

IT 7664-39-3, Hydrofluoric acid, processes
7697-37-2 , *Nitric* *acid* , processes
7664-38-2, *Phosphoric* *acid* , processes
RL: PROC (Process) (copper contamination control in *clean* processes for wafer impurity elimination in optical lithog.)

IT 7647-01-0, Hydrochloric acid, processes

L15 ANSWER 3 OF 23 HCAPLUS COPYRIGHT 2001 ACS
AN 1998:806886 HCAPLUS
DN 130:59907
TI Method of fabricating a semiconductor device, method of *cleaning*

such a device, and *cleaning* agent for this purpose
IN Kordic, Srdjan; Knotter, Dirk Maarten; Mutsaers, Cornelis Adrianus Henricus Antonius
PA Koninklijke Philips Electronics N.V., Neth.; Philips AB

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9856038	A1	19981210	WO 1998-IB567	19980416
EP 929909	A1	19990721	EP 1998-910950	19980416
JP 2000516404	T2	20001205	JP 1998-529407	19980416
PRAI EP 1997-201720	A	19970606	WO 1998-IB567	W 19980416

AB A conductor track or so-called *via* is advantageously provided by a so-called Damascene process in the manuf. of, for example, ICs. The conductive material used often comprises two materials, such as an Al-Cu alloy which is provided in a recess or through *opening* in an insulating layer. First a thick layer of the desired material is provided over the insulating layer and the recess therein. Then the conductive material is removed from outside the recess again by chem.-mech. polishing. This, however, leads to a roughening of the surface of the remaining conductive material which is undesirable. According to the invention, a 1st layer of the 1st material, for example Al, is 1st provided over the insulating layer and the recess therein in such a process. And subsequently part of the 1st layer of the 1st material is removed by a chem. etchant, preferably by chem.-mech. polishing, whereupon a 2nd layer which is thin compared with the 1st layer and which is made of the 2nd material, for example Cu, is provided over the remaining portion of the 1st layer of the 1st material. After which the remaining portion of the 1st layer of the 1st material and the 2nd, comparatively thin layer of the 2nd material are mixed with one another by a thermal treatment. Since the 1st layer comprises only a single material, a conductor track or *via* is thus obtained without the surface thereof being roughened. The invention also relates to a method of *cleaning* an IC which comprises a conductor track or *via* of a material comprising Al, and a *cleaning* agent suitable for this purpose.

IT *7664-38-2* , *Phosphoric* *acid* , processes
7664-39-3, Hydrogen fluoride, processes 7664-93-9, Sulfuric acid, processes *7697-37-2* , *Nitric* *acid* , processes
10028-15-6, Ozone, processes 10043-35-3, Boric acid, processes
RL: NUU (Nonbiological use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (in method of fabricating semiconductor device, method of *cleaning* such device, and *cleaning* agent for purpose)

L15 ANSWER 6 OF 23 HCAPLUS COPYRIGHT 2001 ACS
AN 1995:316221 HCAPLUS
DN 123:45626
TI Method to eliminate corrosion in conductive elements
IN Langley, Rodney C.
PA Micron Semiconductor, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM

DT Patent
LA English
IC ICM H01L021-00
NCL 156664000
CC 76-2 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5376235	A	19941227	US 1993-91542	19930715

AB A semiconductor wafer is washed in a dil. H3PO4 soln. after the metal features have been patterned and etched, thereby removing substantially all of the *residual* oxide, Cl, and/or F contamination which remains on the features. This will substantially eliminate corrosion of the features. The H3PO4 wash also substantially prevents voids from forming during a subsequent alloying step. The features can include bond pads, *vias* , *contacts* , and interconnects.
IT *7664-38-2* , *Phosphoric* *acid* , processes
7757-79-1, *Nitric* *acid* potassium salt, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(in removal of contaminants from semiconductor wafers to prevent corrosion of conductive elements)

L15 ANSWER 7 OF 23 HCAPLUS COPYRIGHT 2001 ACS
AN 1994:21555 HCAPLUS
DN 120:21555
TI Manufacture of semiconductor devices with multilayered aluminum wiring
IN Myazaki, Taichi
PA Citizen Watch Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-90
ICS H01L021-3205
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05235176	A2	19930910	JP 1992-73157	19920225

AB In the title manuf., a semiconductor substrate is coated with 1st Al wiring (a), interlayer insulator (b), and resist layers (c) in that order; c is patterned; b is dry-etched utilizing c as a mask to form through *holes* ; c is ashed in O plasma; the substrates are dipped in mixt. of H3PO4, AcOH, HNO3, and ammonium fluoride; and then a 2nd Al wiring are formed. The Al circuit paths are completely connected *via* through *holes* .
IT 64-19-7, Acetic acid, uses *7664-38-2* , *Phosphoric* *acid* , uses *7697-37-2* , *Nitric* *acid* , uses 12125-01-8, Ammonium fluoride
RL: USES (Uses)

(treatment with, of through *holes* , in forming multilayered aluminum circuits in semiconductor device fabrication)

L15 ANSWER 11 OF 23 WPIX COPYRIGHT 2001 DERWENT INFORMATION LTD
AN 2000-442203 [38] WPIX
DNN N2000-330010 DNC C2000-134386
TI Method for rinsing metallized semiconductor substrates involves contacting with aqueous medium and anticorrosive agent(s) such as organic and/or inorganic acids at controlled concentration for preset time.
DC E19 L03 U11
IN FAHRENKRUG, J; LINDQUIST, P G; OLSON, C R; ROSATO, J J
PA (SCPG-N) SCP GLOBAL TECHNOLOGIES DIV PRECO INC
CYC 89
PI WO 2000034998 A1 20000615 (200038)* EN 54p H01L021-3213
AU 2000020428 A 20000626 (200045) H01L021-3213
ADT WO 2000034998 A1 WO 1999-US28877 19991203; AU 2000020428 A AU 2000-20428 19991203
FDT AU 2000020428 A Based on WO 200034998
PRAI US 1999-408279 19990929; US 1998-111287 19981207; US 1999-133326 19990510
IC ICM H01L021-3213
ICS C23F001-16; H01L021-306
AB WO 200034998 A UPAB: 20000811
NOVELTY - A method and system for rinsing of semiconductor substrate such as metallized semiconductor wafer involves contacting the substrate with an aqueous medium and anticorrosive chemical agent(s). The concentration of chemical agent(s) is maintained at a controlled level for a predetermined time.

DETAILED DESCRIPTION - A method for rinsing metallized semiconductor substrate with an aqueous medium which comprises anticorrosive agents selected from organic carboxylic acids, organic nitrogen-containing compounds, inorganic acids other than nitric and carbonic acids and/or carbon monoxide and ozone.

INDEPENDENT CLAIMS are also included for the following:

(1) A system for rinsing a metallized semiconductor substrate comprises a means for contacting the substrate with an aqueous medium containing anticorrosive chemical agent(s). The concentration of the anticorrosive chemical agent(s) is maintained at the controlled level and the substrate is maintained in *contact* with the chemical agent(s) for a predetermined time.

(2) A method for rinsing non-metallized semiconductor substrate involves contacting the substrate with an aqueous medium containing chemical agents selected from hydrofluoric acid, hydrochloric acid, nitrilotriacetic acid and/or EDTA (ethylenediaminetetraacetic acid), gettering agents, chelating agents and surfactants.

USE - For rinsing metallized semiconductor substrates having one or more layers of metal (such as copper or titanium nitride) deposited on them.

ADVANTAGE - The system provides minimal addition of corrosive agent and is relatively compact, inexpensive, efficient and easy to operate.

L15 ANSWER 16 OF 23 WPIX COPYRIGHT 2001 DERWENT INFORMATION LTD
AN 1995-165032 [22] WPIX
DNN N1995-129549 DNC C1995-076223
TI Removal of resist masks - using solution of *nitric* *acid* or *phosphoric* *acid* or mixture of both to perform exposure of selective target substance.
DC G06 L03 U11
IN SHINAGAWA, K
PA (FUIT) FUJITSU LTD
CYC 2
PI JP 07086146 A 19950331 (199522)* 8p H01L021-027
US 5628871 A 19970513 (199725) 14p H01L021-312
ADT JP 07086146 A JP 1993-232018 19930917; US 5628871 A US 1994-264915 19940624
PRAI JP 1993-232018 19930917
IC ICM H01L021-027; H01L021-312
ICS H01L021-3065
AB JP 07086146 A UPAB: 19950609
The removal method involves removal of a resist mask (32) after performing ion implantation through it to a semiconductor wafer (13). Hydrogen is the principal ingredient of a gaseous mixture, which is used for plasma processing of a selective target substance. Then a gaseous mixture containing oxygen is used to perform down flow processing of the target substance.

Then exposure of the target substance is carried by a solution containing either *nitric* *acid* or *phosphoric* *acid* or both.

ADVANTAGE - Removes scum completely. Inhibits resist explosion. Reduces particle generation greatly.

L15 ANSWER 23 OF 23 WPIX COPYRIGHT 2001 DERWENT INFORMATION LTD
AN 1980-29976C [17] WPIX
TI Finely etching a cobalt (alloy) metallic film - by contacting with etching liq. of *nitric* *acid* and *phosphoric* *acid* .
DC M14
PA (SHAF) SHARP KK
CYC 1
PI JP 55034673 A 19800311 (198017)*
JP 60053754 B 19851127 (198551)
PRAI JP 1978-107988 19780831
IC C23F001-00
AB JP 55034673 A UPAB: 19930902
A film of pure Co, Co-P or other Co alloys is contacted with an etching

liquid of *nitric* *acid* and *phosphoric* *acid* in the concn. of *nitric* *acid* 5-70 vol. %. The high viscosity *phosphoric* *acid* restricts the etching liquid from invading clearance between the cobalt film and a resist, and reduces the etching speed to a suitable extent so that amt. of the side edge is decreased to enable the film to be precisely worked with smooth surface as well as sharp stepwise section and without any *residue* formed on other than the patterned portion.

L16 ANSWER 4 OF 34 HCAPLUS COPYRIGHT 2001 ACS
AN 1997:195450 HCAPLUS
DN 126:189656
TI Aluminum alloy castings and surface treatment thereof
IN Kinoshita, Shigeo
PA Shoowa Kk, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM B22D029-00
ICS B22D029-00; B22D021-04; C23F001-20; C23F003-03; C25D011-16; C25D011-18; C25F003-20
CC 56-6 (Nonferrous Metals and Alloys)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09001319	A2	19970107	JP 1995-175663	19950620

AB An Al alloy casting is rubbed to eliminate pin *holes* , blow *holes* , etc., in the surface layer, surface treated e.g., with HF, a F-contg. compd., H3PO4, or HNO3, to remove Si present in the surface chill layer, and successively anodized, colored, and sealed. An anodized film of uniform coloration and gloss can be obtained.
IT *7664-38-2* , *Phosphoric* *acid* , processes
7664-39-3, Hydrofluoric acid, processes *7697-37-2* , *Nitric* *acid* , processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(aluminum alloy castings and surface treatment thereof)

L16 ANSWER 7 OF 34 HCAPLUS COPYRIGHT 2001 ACS
AN 1985:71222 HCAPLUS
DN 102:71222
TI *Cleaning* of oxide films from aluminum pnictides
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent

LA Japanese
IC H01L021-306; H01L021-304
CC 76-3 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 59152632	A2	19840831	JP 1983-28121	19830221
JP 05054259	B4	19930812		

AB The selective removal of oxide films from Group IIIA pnictides contg. Al is achieved by using H3PO4 solns. Thus, the oxide surface layer of p-(Al,Ga)As on GaAs was removed by H3PO4 etching before adding *contacts* .
ST etching surface oxide aluminum IIIA pnictide; *phosphoric* *acid* *cleaning* gallium aluminum arsenide
IT Aluminum pnictides
RL: USES (Uses)
(*cleaning* of oxide films from, with *phosphoric* *acid* solns.)
IT Electric *contacts*
(formation of, on aluminum pnictide surfaces after *cleaning* with *phosphoric* *acid*)
IT Etching
(of oxide films from aluminum pnictide surfaces with *phosphoric* *acid* solns.)
IT *7664-38-2* , uses and miscellaneous
RL: USES (Uses)
(*cleaning* soln. contg., for aluminum pnictide surfaces)
7697-37-2 ,
uses and miscellaneous 7722-84-1, uses and miscellaneous
RL: USES (Uses)
(in *cleaning* of aluminum pnictide surfaces)

L16 ANSWER 8 OF 34 HCAPLUS COPYRIGHT 2001 ACS
AN 1984:43626 HCAPLUS
DN 100:43626
TI New technologies for metalization of semiconductor devices
AU Chadda, Madan M.; Scheffelmann, Franz; Stoeger, Wolfgang
CS Ges. Gleichrichterbau Elektron. m.b.H., Semikron, Nuernberg, D-8500, Fed. Rep. Ger.
SO Forschungsber. - Bundesminist. Forsch. Technol., Technol. Forsch. Entwickl. (1983), BMFT-FB-T 83-035, 59 pp.
CODEN: BFTEAJ; ISSN: 0340-7608
DT Report
LA German
CC 76-2 (Electric Phenomena)
Section cross-reference(s): 55, 56, 67
AB New methods were studied for the electroless deposition of Al, Ni, Pd, and alloy *contacts* for semiconductor devices. The Al deposition from the decompn. of organometallics was studied for Si, glass, SiO2, Al2O3, Cu, Cr-Ni steel, and Teflon substrates. Catalysts for this

decompn. are Ti-(C2H5)TiCl2, ZrCl4, HfCl4, and UCl3. Ohmic *contacts* are prepd. by heating to form an Al-1.7% Si alloy or depositing Ni on the *cleaned* Al surface. The uses of photomask etching and left-off techniques in patterning the Al *contacts* were investigated. The reductive deposition of Co, Ni, B, and P alloys with W and Mo from NaH2PO2 baths is described with Au catalysts. The Ni deposition on Pb-contg. passiwating glasses was studied. Pd Schottky contracts with Si are prepd. by reductive deposition with tetrachloropalladic acid in baths contg. either amino acids, amino alcs., NaH2PO2, or NH2NH2.H2O. The Pd *contacts* have poor adhesion.

L16 ANSWER 9 OF 34 HCAPLUS COPYRIGHT 2001 ACS
AN 1983:147920 HCAPLUS
DN 98:147920
TI Study of a new acidic *cleaning* agent for anodized aluminum surfaces
AU Broockmann, Karl; Ellwanger, Hans; Osberghaus, Rainer
CS Dieblich/Mosel, Fed. Rep. Ger.
SO Aluminium (Duesseldorf) (1982), 58(11), 650-2
CODEN: ALUMAB; ISSN: 0002-6689
DT Journal
LA German
CC 56-6 (Nonferrous Metals and Alloys)
AB The development and testing of the Midal [85256-33-3] *cleaner* , based on dil. HNO3, phosphonic acid ester, and *phosphoric* *acid* ester mixt., is described. Use of the *cleaner* requires less energy than abrasive *cleaners* , and gives problem-free removal of heavy deposits. Despite the presence of acids, the *cleanser* does not attack anodized Al even on long *contact* .
IT *7664-38-2D* , esters
RL: USES (Uses)
(in *cleaning* soln. for anodized aluminum)
IT *7697-37-2* , properties 13598-36-2D, esters
RL: PRP (Properties)
(in *cleaning* soln. for anodized aluminum)

L16 ANSWER 11 OF 34 HCAPLUS COPYRIGHT 2001 ACS
AN 1977:521408 HCAPLUS
DN 87:121408
TI Evaluation of agents for pickling copper alloy connector parts
AU Piazza, John R.
CS West. Electr. Eng. Res. Cent., Princeton, N. J., USA
SO Plat. Surf. Finish. (1977), 64(1), 41-8
CODEN: PSFMDH
DT Journal
LA English
CC 56-5 (Nonferrous Metals and Alloys)

AB Acidic pickling agents for treating Cu alloy elec. connectors prior to electroplating were evaluated by detg. Ni thickness required to produce low-porosity deposits. Coupons of dual metal sheet (CDA 172 [37373-69-6] and CDA 155 [63142-18-7]) or Cu-4Ni 4% Sn alloy [63982-61-6] sheet were cut, *cleaned* , pickled, and electroplated with 0.5-4.0 .mu. Ni from a sulfamate bath. Wt. loss in pickling, surface topog., and microstructure were assessed. Adherence of plated Ni was detd. by using bend and heat quench tests. Porosity was detd. by using electrog. printing.

IT 64-19-7, reactions 7647-01-0, reactions *7664-38-2* , reactions 7664-93-9, reactions 7681-38-1 *7697-37-2* , reactions 7722-84-1, reactions
RL: RCT (Reactant)
(pickling of copper alloys in solns. contg.)

L24 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2001 ACS
AN 1995:316221 HCAPLUS
DN 123:45626
TI Method to eliminate corrosion in conductive elements
IN Langley, Rodney C.
PA *Micron Semiconductor, Inc., USA*
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-00
NCL 156664000
CC 76-2 (Electric Phenomena)
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5376235	A	19941227	US 1993-91542	19930715

AB A semiconductor wafer is *washed* in a dil. H3PO4 soln. after the metal features have been patterned and etched, thereby removing substantially all of the *residual* oxide, Cl, and/or F contamination which remains on the features. This will substantially eliminate corrosion of the features. The H3PO4 *wash* also substantially prevents voids from forming during a subsequent alloying step. The features can include bond pads, vias, contacts, and interconnects.

IT *7664-38-2* , *Phosphoric* *acid* , processes
7757-79-1, *Nitric* *acid* potassium salt, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(in removal of contaminants from semiconductor wafers to prevent corrosion of conductive elements)

IT 7782-41-4, Fluorine, processes 7782-50-5, Chlorine, processes
RL: REM (Removal or disposal); PROC (Process)
(removal of contaminants from semiconductor wafers to prevent corrosion

of conductive elements)

L30 ANSWER 8 OF 8 INSPEC COPYRIGHT 2001 IEE
AN 1989:3312919 INSPEC DN B89015233
TI Hybrid dry-wet chemical etching process for *via* *holes* for gallium arsenide MMIC manufacturing.
AU Chang, E.Y.; Nagarajan, R.M.; Kryzak, C.J.; Pande, K.P. (Comput. Syst. Div., Unisys Corp., St. Paul, MN, USA)
SO IEEE Transactions on Semiconductor Manufacturing (Nov. 1988) vol.1, no.4, p.157-9. 8 refs.
Price: CCCC 0894-6507/88/1100-0157$01.00
CODEN: ITSMED ISSN: 0894-6507
DT Journal
TC Experimental
CY United States
LA English
AB Through the wafer *via* - *hole* connections for monolithic microwave integrated circuits (MMIC) manufacturing have been developed by combining reactive ion etching (RIE) and wet chemical spray etching processes for 100- mu m-thick gallium arsenide wafers. The dry process is based on the use of SiCl4-BCl3-Cl2 and BCl3-Cl2 gas mixtures at room temperature is a reactive ion etcher. The etching parameters are optimized for anisotropic etching, initially, followed by slightly isotropic etching. To remove the residual 'lip' and surface roughness, following reactive ion etching, a dynamic wet chemical spray etching based on H3PO4-H2O2-H2O at 45 degrees C is used. The combined dry-wet etching approach is used to fabricate <120- mu m diameter *via* - *holes* in 100- mu m-thick GaAs substrates with a wider process latitude. With this process, the authors have achieved >95 percent yield across 3-in wafers. Metallized *via* - *hole* contacts to power FET chips show a contact resistance <20 m Omega per via for 5- mu -thick selective gold plating.
CHI *H3PO4 ss, PO4* ss, H3 ss, O4 ss, H ss, O ss, P ss* ; *H3PO4H2O2H2O ss, PO4 ss, H2 ss, H3 ss, O2* ss, O4 ss, H ss, O ss, P ss*

L36 ANSWER 1 OF 7 INSPEC COPYRIGHT 2001 IEE
AN 2000:6647239 INSPEC DN A2000-16-7340N-006; B2000-08-2530D-022
TI Ohmic *contact* formation mechanism of Pd nonalloyed *contacts* on p-type GaN.
AU Jong-Lam Lee; Jong Kyu Kim (Dept. of Mater. Sci. & Eng., Pohang Univ. of Sci. & Technol., South Korea)
SO Journal of the Electrochemical Society (June 2000) vol.147, no.6, p.2297-302. 21 refs.
Published by: Electrochem. Soc
Price: CCCC 0013-4651/2000/$7.00
CODEN: JESOAN ISSN: 0013-4651
SICI: 0013-4651(200006)147:6L.2297:OCFM;1-S

DT Journal
TC Experimental
CY United States
LA English
AB The surface of p-type GaN was treated with HCl, H3PO4, KOH, and aqua regia solutions before the deposition of Pd metal, and the ohmic *contact* formation mechanism was studied by observing the change of ohmic characteristics with the pretreatment of the surface. *Contact* resistivity decreased in sequence with treatment using HCl, H3PO4, KOH, and aqua regia solutions. The *contact* resistivity on p-type GaN treated with boiling aqua regia was decreased by two orders of magnitude in comparison with the HCl treated one. The amounts of oxygen and carbon atoms on p-type GaN were reduced with the same sequence of surface treatment and the aqua regia solution is most effective in selectively removing surface oxides without etching the p-type GaN. This provides evidence that the reduction of *contact* resistivity originates from the selective removal of surface oxides, acting as an impeding barrier for *hole* injection from metal to p-type GaN.
Contact resistivities did not change when the *hole* concentration was varied from 2.8*1016 to 2.5*1017 cm-3 in both the HCl treated and aqua regia treated samples. This suggests that the formation of ohmic *contact* on p-type GaN can be explained by the thermionic emission of *holes* at the interface of Pd with p-type GaN. The Schottky barrier height deduced from both electron affinity of GaN and work function of Pd is much differ from the value of about 0.35 to 0.45 eV experimentally determined using *contact* resistivities. This proposes that the Fermi level pinning at acceptor-type point defects on the surface of p-type GaN lead to the ohmic *contact* on p-type GaN.
CHI *H3PO4 ss, PO4 ss,

L36 ANSWER 5 OF 7 INSPEC COPYRIGHT 2001 IEE
AN 1992:4243904 INSPEC DN A9221-8630J-043; B9211-8420-042
TI High performance etchant for thinning p+-InP and its application to p+n InP solar cell fabrication.
AU Faur, M.; Faur, M. (Dept. of Electr. Eng., Cleveland State Univ., OH, USA); Bailey, S.; Brinkler, D.; Goradia, M.; Weinberg, I.; Fatemi, N.
SO Conference Record of the Twenty Second IEEE Photovoltaic Specialists Conference - 1991 (Cat. No.91CH2953-8)
New York, NY, USA: IEEE, 1991. p.241-5 vol.1 of 2 vol. 1598 pp. 10 refs.
Conference: Las Vegas, NV, USA, 7-11 Oct 1991
Sponsor(s): IEEE
Price: CCCC CH2953-8/91/0000-0241$01.00
ISBN: 0-87942-636-5
DT Conference Article
TC Practical
CY United States
LA English

AB An etchant, namely (o-H3PO4)u: (*HNO3*)v: (H2O2)t: (H2O)1-(u+v+t) has been developed for thinning, after *contacting* , the p+ emitter layer of p+n InP structures made by thermal diffusion. Varying u, v, and t, reproducible etch rates of 5 to 110 nm/min have been obtained. After thinning the 0.6 to 2.5 mu m thick p+ InP layer down to 60-250 nm, specular surfaces have been obtained at up to 80 nm/min etch rate. Due to its intrinsic qualities the *residual* P-rich oxide after thinning the emitter layer provides surface passivation of p+ InP surfaces and can also serve as a first-layer AR coating.

CHI *H3PO4 ss, PO4 ss, H3 ss, O4 ss, H ss, O ss, P ss* ;*HNO3 ss,* NO3 ss, O3 ss, H ss, N ss, O ss*
HNO3; H*O; H2O2; H3PO; O*P; PO; H; O; HNO; N*O; NO; H2O; In

L36 ANSWER 7 OF 7 INSPEC COPYRIGHT 2001 IEE

AN 1985:2531310 INSPEC DN B85055758

TI A MoSi2 Schottky diode for bipolar LSIs.

AU Vamamoto, Y.; Miyanaga, H.; Amazawa, T.; Sakai, T. (Atsugi Electr. Commun. Lab., NTT Public Corp., Kanagawa, Japan)

SO IEEE Transactions on Electron Devices (July 1985) vol.ED-32, no.7, p.1231-9. 9 refs.
Price: CCCC 0018-9383/85/0700-1231$01.00
CODEN: IETDAI ISSN: 0018-9383

AB Fabrication and characterization of a molybdenum silicide Schottky diode have been investigated for application to bipolar logic LSIs using a Schottky TTL. The diode consists of a silicon (111) n-type substrate, a molybdenum silicide layer, and aluminum with a 2%-silicon electrode that also acts as a first-layer wiring metal in the bipolar LSI. The silicide layer was formed by the reaction of Si substrate and deposited Mo through heat treatment in a nitrogen-gas atmosphere at 550 degrees C for 30 min. It was found that Mo could be selectively and *cleanly* etched by a mixed solution of *phosphoric* acid, *nitric* *acid* , acetic *acid* , and water. The silicide layer is polycrystalline MoSi2 with a hexagonal structure, and the built-in voltage of the diode is 0.68 eV. Thermal stability for the MoSi2 diode with a 2%-Si:Al electrode is good after heat treatment at 500 degrees C for 1 h. In order to apply the Schottky diode to the bipolar LSI fabrication process SST-2, the silicide formation for boron- and arsenic-doped polysilicon was also investigated. The *contact* resistance for the polysilicon-MoSi2-2%-Si:Al *contact* was between 60 and 70 Omega - mu m2 as well as that for the polysilicon-2%-Si:Al *contact* . By using this diode 1-kbit RAMs and 16K gate logic LSI were fabricated with high yield.